CLAIMS

What is claimed is:

1. A method of deriving heat flux data for a workpiece having a top surface and a bottom surface in a process chamber for a temperature sensitive process, the process chamber includes a support for supporting the bottom surface of the workpiece and regulating the temperature of the workpiece, the process includes using at least two process parameters activated for an amount of time, the method being performed using a sensor apparatus for measuring temperature data, processing, storing, and transmitting the temperature data, the sensor apparatus having at least one temperature sensor, an information processor, a memory for storing information, a wireless information transmitter, a wireless information receiver, and a base for supporting the sensor, the information processor, the memory, the information transmitter, and the information receiver, the method comprising the steps of:

A. loading the sensor apparatus into the process chamber;

B. collecting and storing non-process temperature data using the sensor apparatus with all of the at least two process parameters turned off;

C. collecting and storing separate parameter process temperature data using the sensor apparatus with each of the at least two process parameters separately activated;

D. collecting and storing combined parameter process temperature data using the sensor apparatus with all of the at least two process parameters for processing the workpiece jointly activated; and

E. calculating the heat flux into and out of the workpiece using temperatures measured in steps B-D and intrinsic thermal properties of the workpiece.

2. The method of claim 1 wherein the workpiece comprises a semiconductor wafer for fabricating electronic devices, a substrate for a lithography mask, or a substrate for a flatpanel display.

3. The method of claim 1 wherein the temperature sensitive process is selected from the group consisting of plasma etching, plasma deposition, plasma enhanced chemical vapor deposition, chemical vapor deposition, and sputter deposition.

4. The method of claim 1 wherein the workpiece comprises a semiconductor wafer for fabricating electronic devices and wherein the temperature sensitive processincludes a plasma etching process.

5. The method of claim 1 wherein the workpiece comprises a flat panel display substrate and wherein the temperature sensitive process includes a plasma etching process.

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6. A method of maintaining a process chamber for performing a temperature sensitive process on a semiconductor wafer, the process chamber includes a support for supporting the bottom surface of the wafer and regulating the temperature of the wafer, the method comprising the steps of:

A. providing target heat flux values, F_T, for heat flux into and out of the wafer for predetermined conditions;

B. making new measurements of temperatures experienced by the semiconductor wafer for the predetermined conditions;

C. deriving new heat flux values, F_N, using the temperatures from step B;

D. comparing the target heat flux, F_T, to the new heat flux, F_N, to assign a status for the process chamber so that the process chamber status is

operational if F_T and F_N are substantially equal or

malfunctioning if F_T and F_N are not substantially equal.

7. The method of claim 6 wherein F_T represents a target heat flux for the top surface of the wafer and a target heat flux for the bottom surface of the wafer and F_N represents a new heat flux for the top surface of the wafer and a new heat flux for the bottom surface of the wafer wherein the top surface heat flux and the bottom surface heat flux each correspond to a separate operating parameter for the process chamber and step B further comprising comparing the target heat flux and new heat flux for each operating parameter for the process chamber.

8. The method of claim 6 wherein the temperature sensitive process is selected from the group consisting of plasma etching, plasma deposition, plasma enhanced chemical vapor deposition, chemical vapor deposition, and sputter deposition.

9. The method of claim 7 wherein the top surface heat flux results from a glow discharge plasma.

10. The method of claim 6 wherein step A comprises deriving heat flux values for the wafer, the temperature sensitive process includes using at least two process parameters activated for an amount of time, step A being performed using a sensor apparatus for measuring temperature data, processing, storing, and transmitting the temperature data, the sensor apparatus having at least one temperature sensor, an information processor, a wireless information transmitter, and a base for supporting the sensor, the information processor, the memory, the information transmitter, and the information receiver, step A comprising the steps of:

i. loading the sensor apparatus into the process chamber;

ii. collecting and storing non-process temperature data using the sensor apparatus with all of the at least two process parameters turned off;

iii. collecting and storing separate parameter process temperature data using the sensor apparatus with each of the at least two process parameters separately activated;

iv. collecting and storing combined parameter process temperature data using the sensor apparatus with all of the at least two process parameters for processing the wafer jointly activated; and

v. calculating the heat flux into and out of the workpiece using temperatures measured in steps ii-iv and intrinsic thermal properties of the wafer.

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11. A method of operating a manufacturing facility for processing wafers using temperature sensitive processes, the method comprising the steps of:

A. providing at least one process chamber capable of processing the wafers, wherein the process chamber is part of the manufacturing facility;

B. providing a sensor apparatus for measuring temperatures experienced by the wafer and capable of wirelessly collecting and transmitting or storing temperature data from within the process tool;

C. providing target heat flux values, F_T , for heat flux into and out of the wafer for predetermined conditions;

D. making new measurements of temperatures experienced by the semiconductor wafer for the predetermined conditions;

E. deriving new heat flux values, F_N , using the temperatures from step D;

F. comparing the target heat flux, F_T , to the new heat flux, F_N , to assign a status for the process chamber so that the process chamber status is

i. operational if F_T and F_N are substantially equal or

ii. malfunctioning if F_T and F_N are not substantially equal .

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12. A computer readable medium encoded with computer executable steps for deriving heat flux values for managing a plasma process chamber, the chamber being capable of generating a plasma, the chamber having a chuck for supporting a workpiece in the plasma, at least one of the heat flux values being a plasma heat flux, at least one of the heat flux values being a chuck heat flux, the steps comprising:

A. obtaining temperature meausurements, T(x,y,t), representing the temperature of the workpiece in the chamber in the presence of the plasma;

B. using the temperature measurements, T(x,y,t), to compute the within workpiece thermal flux term $\nabla^2 T(x, y, t)$ using the equation

$\nabla^2 T(x,y,t)$ = Average of T over a circle of small radius centered at (x,y) – T(x,y,t) ;

C. estimating the chuck temperature, T_c , and the chuck conduction coefficients, α, for spatial co-ordinates (x,y) by determining a best fit of the temperature measurements to the equation

$$\frac{dT}{dt} = k_w \nabla^2 T - k_c \alpha (T - T_c) \text{ ; and}$$

D. computing the plasma heat flux, Φ_p , and the chuck heat flux, Φ_c , using the equations

$$\Phi_c = \alpha (T - T_c) \qquad \text{and}$$

$$k_p \Phi_p = \frac{dT}{dt} - k_w \nabla^2 T + k_c \Phi_c .$$

13. The medium of claim 12 werein step A comprises retrieving temperature measurements from a memory storing the temperature measurements, retrieving

temperature measurements from an information transfer interface, or retrieving temperature measurements via a connection with a temperature measuring device.

14. The medium of claim 12 werein step B comprises spatially interpolating the temperatures T onto a fine spatial grid.

15. The medium of claim 12 werein step B comprises spatially interpolating the temperatures T onto a fine spatial grid using standard Kriging methods or linear interpolation methods based on a Delaunay triangulation.

16. The medium of claim 12 werein step C comprises determining the chuck temperature T_c and the chuck conduction coefficients α by minimizing the Euclidean metric

$$\min\left\|\frac{dT}{dt} - k_w\nabla^2 T + k_c\alpha(T - T_c)\right\|$$

using a least squares procedure.

17. The medium of claim 12 werein the workpiece comprises a semiconductor wafer.

18. The medium of claim 12 werein the workpiece comprises a semiconductor wafer, a flat panel display substrate, or a lithography mask.

19. The medium of claim 12 werein step B comprises spatially interpolating the temperatures T onto a fine spatial grid and step C comprises determining the chuck temperature T_c and the chuck conduction coefficients α by minimizing the Euclidean metric

$$\min\left\|\frac{dT}{dt} - k_w\nabla^2 T + k_c\alpha(T - T_c)\right\|$$

using a Least Squares procedure.

20. The medium of claim 12 werein step A comprises retrieving temperature measurements from a memory storing the temperature measurements, retrieving temperature measurements from an information transfer interface, or retrieving temperature measurements via a connection with a temperature measuring device and step B comprises spatially interpolating the temperatures T onto a fine spatial grid using standard Kriging methods or linear interpolation methods based on a Delaunay triangulation.

21. The medium of claim 12 werein step A comprises retrieving temperature measurements from a memory storing the temperature measurements, retrieving temperature measurements from an information transfer interface, or retrieving temperature measurements via a connection with a temperature measuring device; wherein step B comprises spatially interpolating the temperatures T onto a fine spatial grid using standard Kriging methods or linear interpolation methods based on a Delaunay triangulation; wherein step C comprises determining the chuck temperature T_c and the chuck conduction coefficients α by minimizing the Euclidean metric

$$\min\left\|\frac{dT}{dt} - k_w\nabla^2 T + k_c\alpha(T - T_c)\right\|$$

using a least squares procedure; wherein the workpiece comprises a semiconductor wafer; and wherein the workpiece comprises a semiconductor wafer, a flat panel display substrate, or a lithography mask.